Amendments to the Titl :

Amend the title as follows:

~~SERIAL-TO-PARALLEL/PARALLEL-TO-SERIAL CONVERSION ENGINE~~ SYSTEM AND METHOD FOR SERIAL-TO-PARALLEL AND/OR PARALLEL-TO-SERIAL DATA CONVERSION

Amendm nts to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-8 (canceled)

Claim 9 (new): A method for performing serial data to parallel data conversion, the method comprising:

serially receiving a data word at a serial data input interface;

providing said received data word to a serial-to-parallel mapping circuit;

partitioning said provided received data word into a plurality of partitioned received data words;

generating memory write control signals and memory write address signals;

directing said generated memory write control signals and said generated memory write address signals to a memory device;

writing said partitioned provided received data words to said memory device in response to said directing;

generating memory read control signals and memory read address signals;

directing said memory read control signals and said memory read address signals to said memory device;

reading an output data word from said memory device in response to said directing said direct said memory read control signals and said memory read address signals; and

reordering bits of said output data word to provide a parallel output data word.

Claim 10 (new): The method of claim 9 wherein said partitioning is performed by said serial-to-parallel mapping circuit.

Claim 11 (new): The method of claim 9 wherein said generating said memory write control signals and said memory write address signals is performed by said serial-to-parallel mapping circuit.

Claim 12 (new): The method of claim 9 wherein said directing said generated memory write control signals and said generated memory write address signals comprises directing said signals to a first port of said memory device.

Claim 13 (new): The method of claim 9 wherein said writing said partitioned provided received data words comprises:

writing said partitioned provided received data words to uniquely associated memory addresses in said memory device.

Claim 14 (new): The method of claim 9 wherein said directing said memory read control signals and said memory read address signals to said memory device comprises directing said signals to a second port of said memory device.

Claim 15 (new): The method of claim 9 wherein said reading an output data word from of said memory device comprises:

reading said output data word with an output mapping circuit.

Claim 16 (new): The method of claim 9 wherein said reordering said bits of said output data word comprises:

mapping interconnects between an output port of an output mapping circuit and an input port of a parallel output interface.

Claim 17 (new): The method of claim 9 further comprising:

providing a clock rate for said serial-to-parallel mapping circuit which is at least eight times faster than a clock rate for said serial data input interface.

Claim 18 (new): A method for conducting parallel data to serial data conversion, the method comprising:

receiving a parallel data word;

reordering at least one bit of said received parallel data word to provide a reordered parallel data word;

writing said reordered parallel data word to a memory device;

reading output data from said memory device;

partitioning said read output data into a plurality of serial data words; and

providing a serially converted output data word from said plurality of partitioned serial data words.

Claim 19 (new): The method of claim 18 wherein said receiving said parallel data word comprises:

receiving said parallel data word at a parallel-to-serial input mapping circuit.

Claim 20 (new): The method of claim 18 wherein said reordering comprises:

reordering said received parallel data word at a parallel-to-serial input mapping circuit.

Claim 21 (new): The method of claim 18 wherein said writing comprises:

writing said reordered received parallel data word to a first port of said memory device.

Claim 22 (new): The method of claim 18 wherein said reading comprises:

reading data from a second port of said memory device.

Claim 23 (new): The method of claim 18 wherein said reordering comprises:

mapping interconnects between a parallel-to-serial input mapping circuit and said memory device.

Claim 24 (new): A method for performing serial data to parallel data conversion, the method comprising:

serially receiving a data word at a serial data input interface;

partitioning said received data word into a plurality of partitioned received data words;

writing said partitioned received data words to a memory device;

reading an output data word from said memory device; and

reordering at least one bit of said output data word to provide a parallel output data word.

Claim 25 (new): The method of claim 24 wherein said reordering comprises:

mapping interconnects between an output port of an output mapping circuit and an input port of a parallel output interface.

Claim 26 (new): The method of claim 24 wherein said reordering comprises:

reordering said at least one bit of said output data word during communication of said output data word between two connected digital logic devices.

Claim 27 (new): The method of claim 24 wherein said reordering comprises:

mapping interconnects between two connected digital logic devices.

Claim 28 (new): A serial-to-parallel and parallel-to-serial converter comprising:

a serial data input interface for receiving a serial input data word;

an input memory connected to said serial data input interface and responsive to said receiving to convert said serial input data word into a parallel output data word, said input memory including a first memory device having a two memory banks, which two memory banks allow writing of data to a first of said two memory banks simultaneous with reading of data from a second of said two memory banks;

serial communication lines coupled to said input memory and operative to output said parallel output data word onto a parallel data bus;

an output memory operative to receive a parallel input data word from said parallel data bus and to convert said received parallel input data word into a plurality of serial data words, said output memory including a second memory device; and

a serial data output interface for receiving said plurality of serial data words and for providing a serially converted output data word.

Claim 29 (new): The converter of claim 28 wherein said input memory comprises:

a serial-to-parallel mapping circuit responsive to said receiving to provide write control signals and write address signals to said first memory device.

Claim 30 (new): The converter of claim 28 wherein said input memory comprises:

an output mapping circuit in communication with said first memory device;

a parallel output interface; and

a connection between said output mapping circuit and said parallel output interface, said connection mapping interconnects between an output port of said output mapping circuit and an input port of said parallel output interface.

Claim 31 (new): The converter of claim 30 wherein said connection mapping said interconnects is operative to reorder at least one bit of an output data word from said first memory device to provide said parallel output data word.

Claim 32 (new): The converter of claim 28 wherein said second memory device includes two second-memory-device memory banks, which two memory banks allow writing of data to a first of said two second-memory-device memory banks simultaneous with reading of data from a second of said two second-memory-device memory banks.

Amendments to the Abstract:

Amend the Abstract as follows:

~~A serial-to-parallel/parallel-to-serial conversion engine provides a bi-directional interface between a serial TDM highway and a parallel TDM highway. The conversion engine includes a serial-to-parallel data conversion device receives a serially received data word and provides a parallel output data word. The conversion engine includes a serial data input interface that receives the serially received data word and provides a received data word. A serial-to-parallel mapping circuit receives the received data word and generates memory write control and write address signals. A memory device includes a first port responsive to the memory write control signals and write address signals for writing the received data word into the memory device, and a second port responsive to memory read control and read address signals for reading data from the memory device. Output interface circuitry generates the memory read control and read address signals, and receives output data from the memory device and reorders the bits of the parallel output data to provide the parallel data word. The conversion engine also includes a parallel-to-serial conversion device that receives a parallel received data word and provides a serial data word. The parallel-to-serial conversion device includes a memory device having a first port responsive to memory write control and write address signals, and a second port responsive to memory read control and read address signals. A parallel-to-serial mapping circuit receives the parallel received data word and generates the memory write control and write address signals to write a bit shuffled version of the parallel received data word into the memory device. A data output interface generates the memory read control and read address signals to perform reads from the memory device and receives output data from the memory device to provide the serial data word.~~ A system and method for performing serial data to parallel data conversion, the method comprising serially receiving a data word at a serial data input interface; partitioning said received data word into a plurality of partitioned received data words; writing said partitioned provided received data words to a memory device in response to said directing, the memory device having two memory banks, the two memory banks permitting simultaneous writing to and reading from the memory device; reading an output data word from said memory device; and reordering at least one bit of said output data word to provide a parallel output data word.

REMARKS

In the instant amendment, claims 1-8 have been canceled, and new claims 9-32 have been added. Thus, claims 9-32 are pending in this application. The title and abstract have been amended. The new claims, new title, and new abstract are fully supported by Applicant's original disclosure. Should you have any questions regarding the above, please feel free to give the below-listed attorney a call. If additional fees are required, please debit our Deposit Account No. 04-1414.

Respectfully submitted,

DORR, CARSON, SLOAN & BIRNEY, P.C.

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By: Leslie Garmaise

Leslie S. Garmaise
Reg. No. 47,587
3010 East 6th Avenue
Denver, Colorado 80206
(303) 333-3010

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